Notice of Allowability	Application No.	Applicant(s)	
	10/802,590	STARR ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response filed 3/22/05*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *17 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 1-20 are allowed.

2. The following is an examiner's statement of reasons for allowance: the claims recite an integrated MOS circuit stabilized by monitoring changes that affect circuit transistor operation and by compensating for those changes using power supply adjustments. Changes in operating temperature and threshold voltage changes in MOS transistors due to age are measured. Differential measurements are made in which threshold voltages measured in continuously biased monitoring circuits are compared to threshold voltages measured in intermittently biased monitoring circuits. Monitoring and compensation circuitry on the integrated circuits use analog-to-digital and digital-to-analog converters controlled by a control unit to make temperature and threshold voltage measurements and corresponding compensating changes in power supply voltages. Monitoring and compensating for changes in threshold voltage of MOS transistors due to age has not been shown in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McPartland disclose applying high column segment voltages needed to erase and program (write) in a segmented column flash EEPROM memory. Low voltage CMOS

transistors are used for both the read column precharge path and the write/erase data transfer path. Also, the column segment select switch can be constructed of a single, low voltage, n-channel, transistor, rather than two complementary high voltage transistors. All of the above reduces precharge and discharge time, increasing the read speed of the memory. This also eliminates the lengthening of precharge time that occurs as the characteristics of high voltage transistors degrade with age. The present invention provides the additional advantage of eliminating the need to use less reliable high voltage transistors in certain off-pitch circuits needed for write and erase functions, thus increasing overall chip reliability.

Khan disclose an integrated circuit storing multiple bits per memory cell. The amount of charge stored in a memory cell corresponds the multiple bits in a memory cell. Dual banks of shift registers are alternately coupled to one or more data pins and to the memory cells of the memory array speed data transfer for reading and writing operation. Reading is performed in the voltage mode to conserve power. During writing operations, reading of a memory cell is performed in the voltage mode to determine whether the desired programming of the memory cell has been achieved. During the reading of a memory cell, the voltage corresponding to the amount of charge stored in a memory cell is compared against a binary search sequence of reference voltages to determine the multiple bits stored in the memory cell.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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